**Amendments to the Claims**

1(Currently amended). A method for reducing the leakage current through a charge protection device in an integrated circuit, the method comprising:

~~reverse body biasing junction diodes formed by source and drain regions in a bulk region~~ supplying a bulk region of the charge protection device with a first voltage potential through a first device when the integrated circuit is in operation; and

supplying the bulk region with a second voltage potential through a second device when the integrated circuit experiences an electro-static discharge (ESD) event.

2(Currently amended). The method of claim 1, wherein ~~reverse body biasing the charge protection device~~ supplying a bulk region of the charge protection device with a first voltage potential includes reverse body biasing the charge protection device when the integrated circuit is not experiencing an electro-static discharge event.

3(Currently amended). The method of claim 1, wherein ~~reverse body biasing the junction diodes formed by source and drain regions in the bulk region of the charge protection device~~ supplying a bulk region of the charge protection device with a first voltage potential further comprises:

applying ~~a~~ the first voltage potential to ~~a~~ the bulk region of the charge protection device that is higher than a the second voltage potential ~~of the source region~~.

4(Cancelled).

5(Cancelled).

6(Currently amended). An apparatus comprising:

an integrated circuit;

a charge protection device coupled to the integrated circuit; ~~and~~

a resistive element ~~adapted~~ to supply a reverse bias to a bulk region of the charge protection device during normal operation of the integrated circuit; and

another device to supply the bulk region with a voltage potential that compensates the reverse bias when the integrated circuit receives an electro-static discharge (ESD) event.

7(Currently amended). The apparatus of claim 6, wherein the charge protection device comprises a first transistor having a source region and a the bulk region, the resistive element being coupled to the bulk region of the transistor.

8(Original). The apparatus of claim 7, wherein the first transistor comprises a p-channel transistor.

9(Canceled).

10(Canceled).

11(Original). The apparatus of claim 6, wherein the resistive element comprises an n-channel transistor.

12(Canceled).

13(Original). The apparatus of claim 6, wherein the integrated circuit comprises a logic transistor having a gate oxide, and the resistive element comprises a transistor having a gate oxide that is thicker than the gate oxide of the logic transistor.

14(Original). The apparatus of claim 7, wherein the first transistor has a width of at least 500 microns, a channel length of less than about 0.2 microns, and is adapted to conduct at least 1 pulsed amp.

15(Currently amended). An apparatus comprising:

an integrated circuit;

a charge protection device coupled to the integrated circuit, the charge protection device comprising a first transistor and a second transistor, wherein the first transistor and the second transistor are arranged in series; ~~and~~

a buffer having an output coupled to a gate terminal of the first transistor;

a resistive element having a control terminal coupled to the output of the buffer and providing a signal to a gate terminal of the second transistor;

and

a voltage divider ~~adapted to apply~~ includes serially connected transistors to supply a voltage potential to an input of the buffer ~~a gate terminal of the first transistor that is lower than a power supply voltage potential~~.

16(Canceled).

17(Canceled).

18(Currently amended). An apparatus comprising:

a first transistor coupled between a positive power conductor and a ground power conductor to provide charge protection for an integrated circuit; ~~and~~

a resistive element coupled to provide a bulk region of the first transistor with a voltage potential that is greater than a voltage potential supplied on the positive power conductor; and

a second transistor to couple the voltage potential supplied on the positive power conductor to the bulk region of the first transistor when the integrated circuit experiences an electro-static discharge (ESD) event.

19(Canceled).

20(Canceled).

21(Currently amended). The apparatus of claim ~~19~~ 18, wherein the resistive element comprises a third transistor.

22(Currently amended). The apparatus of claim ~~19~~ 18, wherein the resistive element comprises a third transistor that has a gate oxide that is thicker than a gate oxide of the first transistor.